II. Amendments to the Specification:

Please replace the full paragraph beginning at line 9 on page 1 of the specification with the following paragraph:

--In MOS devices, such as high voltage lateral diffused metal-oxide semiconductor (HVLDMOS) structures, the gate electrode typically may overlap the non-active region due to processing and design issues. When a high enough voltage is applied to the gate, a channel in the non-active region may open up, allowing a leakage current to flow through it, which causes the device's current ~~vs.voltage~~ vs. voltage response to deviate from the desired linear relationship.

Please replace the full paragraph beginning at line 1 on page 8 of the specification with the following paragraph:

--Further embodiments may also provide a transistor device. Transistor devices include, but are not limited to, LDMOS, VDMOS, other types of high power MOS transistors, Fin structure ~~fieled~~ field effect transistors (FinFET), and strained MOS structures.

This listing of claims will replace all prior versions, and listings, of claims in the application:

III. Listing of Claims:

1. (Canceled)

2. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 further comprising:

the source having a second edge and the drain having a second edge;

the gate having a second portion; and

a second deep trench structure located under the second portion of the gate and proximate to the second edge of the source and the second edge of the drain.

3. (Currently amended) The semiconductor device of claim 2 wherein the first edge of the source and drain are approximately parallel to the second edge of the source and drain, and wherein the first and second deep trench structures are approximately parallel to the first and second edges, respectively.

4. (Currently amended) ~~The semiconductor device of claim 1~~ A semiconductor device comprising:

a substrate including a source and drain, the source having a first edge and the drain having a first edge;

a gate between the source and drain, the gate having a first portion; and

a first deep trench structure located directly under the first portion of the gate viewed in a direction from the gate to the substrate, and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure has a depth greater than 0.5 μm.

5. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the first deep trench structure exhibits a geometry selected from the group consisting of a straight line, an angled line, a broken line, and a combination thereof.

6. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 further comprising:

an outside edge on the source;

an outside edge on the drain; and

the first deep trench structure having a length extending at least from the outside edge of the source to the outside edge of the drain.

7. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the first deep trench structure is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof.

8. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the substrate is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof.

9. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the device includes a strained MOS structure.

10. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 further comprising:

a neighboring semiconductor device; and

a first shallow trench isolation structure located between the semiconductor device and the neighboring semiconductor device.

11. (Original) The semiconductor device of claim 10 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench isolation structure.

12. (Original) The semiconductor device of claim 11 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

13. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 further comprising:

a body contact feature adjacent to the source.

14. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the gate includes a gate electrode and a gate dielectric.

15. (Currently amended) The semiconductor device of claim ~~15~~14 wherein the gate electrode is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof.

16. (Currently amended) The semiconductor device of claim ~~15~~14 wherein the gate dielectric is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof.

17. (Currently amended) The semiconductor device of ~~claim 1~~ claim 4 wherein the first deep trench structure extends around the entire device.

18. (Canceled)

19. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 further comprising:

the source having a second edge and the drain having a second edge;

a second portion of the gate electrode extending past the second edge of the source and the second edge of the drain;

a second deep trench structure located under the second portion of the gate electrode and proximate to the second edge of the source and the second edge of the drain.

20. (Original) The semiconductor device of claim 19 wherein the first edge of the source is approximately parallel to the second edge of the source, the first edge of the drain is approximately parallel to the second edge of the drain, the first deep trench structure is approximately parallel to the first edges and the second deep trench structure is approximately parallel to the second edges.

21. (Currently amended) ~~The semiconductor device of claim 18~~ A semiconductor device comprising:

a substrate including a source and drain, the source having a first edge and the drain having a first edge;

a gate electrode on the substrate and between the source and drain, a first portion of the gate electrode extending past the first edge of the source and the first edge of the drain; and

a first deep trench structure located directly under the first portion of the gate electrode viewed in a direction from the gate electrode to the substrate and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure has a depth greater than 0.5 μm.

22. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the first deep trench exhibits a geometry selected from the group consisting of a straight line, an angled line, a broken line, and a combination thereof.

23. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 further comprising:

an outside edge on the source;

an outside edge on the drain; and

the first deep trench having a length extending at least from the outside edge of the source to the outside edge of the drain.

24. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the first deep trench structure is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof.

25. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the substrate is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof.

26. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the device includes a strained MOS structure.

27. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 further comprising:

a neighboring semiconductor device; and

a first shallow trench isolation structure located between the semiconductor device and the neighboring semiconductor device.

28. (Original) The semiconductor device of claim 27 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench

isolation structure.

29. (Original) The semiconductor device of claim 28 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

30. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 further comprising:
a body contact feature adjacent to the source.

31. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 further comprising:
a gate dielectric adjacent to the gate electrode.

32. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the gate electrode is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof.

33. (Original) The semiconductor device of claim 31 wherein the gate dielectric is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof.

34. (Currently amended) The semiconductor device of ~~claim 18~~ claim 21 wherein the first deep trench structure extends around the entire device.

35. (Canceled)

36. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 further comprising:
the source and drain each having a second edge parallel to their respective first edges;
a second portion of the gate electrode extending past the second edges of the source and

the drain;

a second deep trench structure located under the second portion of the gate electrode and proximate to the second edges of the source and the drain.

37. (Currently amended) ~~The semiconductor device of claim 35~~ A semiconductor device comprising:

a substrate having a source and drain, having widths that are substantially equal and each having a first edge substantially located along a common line on the substrate;

a gate electrode on the substrate and between the source and the drain, the gate electrode having a first portion extending past the first edge of the source and the first edge of the drain; and

a first deep trench structure located directly under the first portion of the gate electrode viewed in a direction from the gate electrode to the substrate, the first deep trench structure parallel to the common line on the substrate and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure is substantially deeper than 0.5 μm.

38. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 further comprising:

an outside edge on the source;

an outside edge on the drain; and

the first deep trench structure having a length extending at least from the outside edge of the source to the outside edge of the drain.

39. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 wherein the first deep trench structure is substantially filled in with a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, a high k material, and a combination thereof.

40. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 wherein the substrate is made of a material selected from the group consisting of crystal silicon, polycrystalline silicon, amorphous silicon, germanium, diamond, silicon germanium, silicon carbide, gallium arsenic, indium phosphide, semiconductor on insulator, and a combination thereof.

41. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 wherein the device includes a strained MOS structure.

42. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 further comprising:

a neighboring semiconductor device; and

a first shallow trench isolation structure between the semiconductor device and the neighboring semiconductor device.

43. (Original) The semiconductor device of claim 42 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench isolation structure.

44. (Original) The semiconductor device of claim 43 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

45. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 further comprising:

a body contact feature adjacent to the source.

46. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 further comprising:

a gate dielectric adjacent to the gate electrode.

47. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 wherein the gate electrode is made of a material selected from the group consisting of doped polysilicon, metal, metal alloy, metal silicide, and a combination thereof.

48. (Original) The semiconductor device of claim 46 wherein the gate dielectric is made of a material selected from the group consisting of silicon oxide, silicon oxynitride, a high k material, and a combination thereof.

49. (Currently amended) The semiconductor device of ~~claim 35~~ claim 37 wherein the first deep trench structure extends around the entire device.

50. (Currently amended) A semiconductor device comprising:

a substrate including a first well of a first-type dopant and a second well of a second type dopant, the first well being disposed laterally adjacent the second well;

a source formed in the first well and drain formed in the second well, the source having a first edge and the drain having a first edge;

a gate electrode on the substrate and between the source and drain, a first portion of the gate electrode extending past the first edge of the source and the first edge of the drain;

a current channel located in a region where the gate electrode extends beyond the first edge of the source and the first edge of the drain, the current channel allowing a leakage current to flow in the device; and

a first deep trench structure formed partially in the first well and partially in the second well, located under the first portion of the gate electrode and proximate to the first edge of the source and the first edge of the drain, whereby the first deep trench structure is located close enough to the first edge of the source and the first edge of the drain to substantially eliminate the leakage current flow through the current channel.

51. (Currently amended) A method of manufacturing a microelectronic device, comprising:

forming a substrate including a first well of a first-type dopant and a second well of a second type dopant, the first well being disposed laterally adjacent the second well;

forming a source in the first well and a drain in the second well;

forming a gate between the source and drain; and

forming a deep trench structure partially in the first well and partially in the second well, underlying a portion of the gate and proximate to an edge of the source and drain.

52. (New) A semiconductor device comprising:

a substrate including a first well of a first type dopant and a second well of a second type dopant;

a source disposed in the first well and a drain disposed in the second well, the source having a first edge and the drain having a first edge;

a gate electrode between the source and drain; and

a deep trench structure located directly under the gate electrode, and proximate to the first edge of the source and the first edge of the drain.

53. (New) The semiconductor device of claim 52 wherein the deep trench is proximate to the first edge of the source and the first edge of the drain with a smaller distance relative to a dimension of the source perpendicular to the first edge of the source.

54. (New) The semiconductor device of claim 52 wherein the deep trench is proximate to the first edge of the source and the first edge of the drain with a distance of about 0.5 μm.